

Design and Characterization of All Graphene Configurable Logic Block for FPGA Applications

Sayed Ali Seif Kashani

Hossein Karimiyan Alidash

Department of Electrical and Computer, Kashan University, Kashan, Iran

ABSTRACT

Scaling and making faster devices are the crucial need in developing technology. The International Technology Roadmap for Semiconductor (ITRS) on the other hand predicts some serious and severe challenges in scaling process of Silicon based devices. Hence, to overcome these challenges, the researchers are actively searching for the new methods and materials. Based on the researches, Carbon based devices are dominant candidate for Silicon based ones.

In this paper Graphene, the Carbon based structure, is chosen to design and characterize the Configurable Logic Block (CLB) as the part of a Field Programmable Gate Arrays (FPGAs). Additionally, CLB's circuit design needs some useful logic devices such as: D-Flip Flop (DFF) and Latch. Following paper presents design and timing characterization of CLB and all of its internal devices and then shows that Graphene based DFF presents about 58 times faster response than its Silicon based counterpart.

Keywords: Configurable Logic Block (CLB), Graphene, Flip Flop, Timing Parameter, Reconfigurable Gate.