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A Low-Power Redundant Decimal Adder: Design and Implementation

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ABSTRACT

In the all computer systems, the add operation is an essential part of all computations and operational processes, hence an overall performance efficiency is achievable by increasing the speed of addition. In conventional number systems, the carry propagation causes a dependency between execution time and the operands' length. This issue can be problematic in high-precision operations and it imposes a long delay.
However, by use unconventional redundant number systems, carry free addition is possible. In redundant number system, add operation can be done in constant time. In this paper, according to the importance of decimal computing systems, a new addition algorithm is proposed for redundant decimal numbers. In the suggested algorithm, by using weighted bits set representation and an effective partitioning, the power dissipation and area consumption are decreased without delay penalty.

Keywords: Decimal Addition, Redundant Representation, Signed Digit, Carry Propagation.