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A New Energy-Aware Mapping and Scheduling Algorithm for Multi-Core Structure

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ABSTRACT

Chips can contain hundreds of pre-designed processing core being into a chip and have provided a chip with high complexity. In the case of such chips, as one of the most important issues is resources mapping and scheduling on the chip. It is well known that the mapping and scheduling tasks is an *NP* problem and need to be controlled together to achieve the effective scheduling and mapping. This paper obtains the solution near to the optimal of static tasks and communications mapping and scheduling in network on chip with two-dimension almesh architecture. The solution is an energy-aware heuristic algorithm, using a combination of genetic algorithm and simulated annealing which aims to minimize energy consumption and the implementation time of an application. Experimental results of some real and standard benchmarks show that the model proposed by this research provides average improvement of about %10in scheduling and improvement of more than %90 in execution time in mapping with relation to genetic algorithm

Keywords: Network on Chip (NoC), Mapping and Scheduling, Genetic Algorithm (GA), Simulated Annealing (SA), Integer Linear Programming (ILP).